module p6(O1, O2, I1, I2, I3);

output O1, O2;

input I1, I2, I3;

nor nor1(nor1\_o, I1, I2);

nand nand1 (nand1\_o, I1, I2);

not not1 (inv\_I3, I3);

not not2 (inv\_inv\_I3, inv\_I3);

not not3 (inv\_nand1\_o, nand1\_o);

not not4 (inv\_inv\_inv\_I3, inv\_inv\_I3);

nor nor2(nor2\_o, inv\_nand1\_o, nor1\_o);

or or1(or1\_o, nor1\_o, inv\_inv\_inv\_I3);

xor xor1(xor1\_o, nor2\_o, inv\_inv\_I3);

nand nand2(O1, nand1\_o, or1\_o);

not not5(O2, xor1\_o);

endmodule

module tb\_p6();

reg I1, I2, I3;

wire O1, O2;

p6 UUT (O1, O2, I1, I2, I3);

initial

begin

I3 = 1'b0;

I2 = 1'b0;

I1 = 1'b0;

#10;

I3 = 1'b0;

I2 = 1'b0;

I1 = 1'b1;

#10;

I3 = 1'b0;

I2 = 1'b1;

I1 = 1'b0;

#10;

I3 = 1'b0;

I2 = 1'b1;

I1 = 1'b1;

#10;

I3 = 1'b1;

I2 = 1'b0;

I1 = 1'b0;

#10;

I3 = 1'b1;

I2 = 1'b0;

I1 = 1'b1;

#10;

I3 = 1'b1;

I2 = 1'b1;

I1 = 1'b0;

#10;

I3 = 1'b1;

I2 = 1'b1;

I1 = 1'b1;

#10;

end

initial

begin

$monitor("I3 = %b, I2 = %b, I1 = %b, O1 = %b, O2 = %b, time = %t \n", I3, I2, I1, O1, O2, $time);

end

endmodule

